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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/015,169 | 10/23/2001 | Ken Kawahata | 9281-4195 | 3270 |

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| EXAMINER | |
|---|---|
| ANYASO, UCHENDU O | |
| **ART UNIT** | **PAPER NUMBER** |
| 2675 | |

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/015,169 | KAWAHATA ET AL. | |
| | Examiner | Art Unit | |
| | Uchendu O Anyaso | 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. **Claims 1-41** are pending in this action.

### *Claim Rejections - 35 USC ' 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1, 2, 4-20, 25-29, 32** and **35-37** are rejected under 35 U.S.C. 102(e) as being anticipated by *Kay* (U.S. 6,175,352).

Regarding **independent claims 1, 25** and **32,** and for **claims 10** and **15,** Kay teaches a shift register circuit comprising: a first shift register 21 having a plurality of stages connected in cascade (figure 1 at 21) and a second shift register 12 having more stages than the first shift register (figure 1 at 12, 21, column 3, lines 9-17).

Furthermore, Kay teaches how the stages of the second shift register 12 are divided into groups (see figure 1 at $13_1$ through $13_m$) each formed of consecutive stages, and the stages of the first shift register 21 are configured to transmit output pulse sequences via switching elements $19_2$ to $19_m$ having a predetermined number of consecutive pulses and having different phases ($\phi 1$, $\phi 2$) from each other, to the stages constituting the groups of the second shift register as clock signals $\phi 1$ and $\phi 2$ (column 3, lines 11-40, figure 1 at 12, 21, $19_2$ to $19_m$, $\phi 1$ and $\phi 2$).

Regarding **claim 2,** in further discussion of claim 1, Kay teaches how the first shift register has an input terminal 22 configured to receive a pulse sequence having a finite number of consecutive pulses (figure 1 at 22, column 3, lines 36-41).

Regarding **claim 4,** in further discussion of claim 2, Kay teaches a plurality of the second shift registers is provided (figure 1 at 12, 21, column 3, lines 9-17).

Regarding **claims 5, 11** and **16,** in further discussion of claim 1, Kay teaches an active matrix circuit having switching devices associated with intersections of signal lines and scanning lines, the scanning lines configured to receive outputs of the stages of the second shift register as scanning signals (column 1, lines 59-67; column 2, lines 9-15; column 3, lines 6-11, figure 1).

Regarding **claims 6-8, 12-14** and **17-19,** in further discussion of claim 5, 11 and 16, Kay teaches how the second shift register comprising MIS transistors of the same type (see figures 2, 3; column 4, lines 6-15).

Regarding **claims 9** and **26-28,** in further discussion of claims 1, 2 and 25, Kay teaches how each stage of the second shift register 12 has clock input terminals (see figure 1 at $\phi 1$ & $\phi 2$,16, 17,$13_1$) configured to receive n-phase (n is an integer of at least two) clock signals ($\phi 1$, $\phi 2$) (see figure 1 at $\phi 1$, $\phi 2$ at of $13_1$, 16, 17).

Furthermore, Kay teaches how an input terminal 14 is configured to receive a signal sent from an input terminal of the second shift register 12 and from an output terminal of a previous stage $13_1$ (figure 12-14).

Also, Kay teaches how an output terminal of shift register $13_1$ is configured to output a signal to one of to an input terminal of a subsequent stage $13_2$ and to an output terminal $11_1$ of the second shift register 12 (figure 1 at $11_1$, $13_1$, $13_2$).

Furthermore, Kay teaches how an initial-stage level is configured to initialize a state of each stage of the second shift register 24 input to a selected stage at one of the clock input terminals ($\phi$1, $\phi$2) (see column 4, lines 16-33, figures 1, 4 at $\phi$1, $\phi$2, of $13_1$, 16, 17).

Regarding **claim 20,** in further discussion of claim 1, Kay teaches Kay teaches how the stages of the second shift register 12 are divided into groups (see figure 1 at $13_1$ through $13_m$) each formed of consecutive stages, and the stages of the first shift register 21 are configured to transmit output pulse sequences via switching elements $19_2$ to $19_m$ having a predetermined number of consecutive pulses and having different phases ($\phi$1, $\phi$2) from each other, to the stages constituting the groups of the second shift register as clock signals $\phi$1 and $\phi$2 (column 3, lines 11-40, figure 1 at 12, 21, $19_2$ to $19_m$, $\phi$1 and $\phi$2).

Regarding **claim 29,** in further discussion of claim 25, Kay teaches a shift register circuit comprising: a first shift register 21 having a plurality of stages connected in cascade (figure 1 at 21) and a second shift register 12 having more stages than the first shift register (figure 1 at 12, 21, column 3, lines 9-17).

Regarding **claim 35,** in further discussion of claim 32, Kay teaches how the clock lines on a thin film transistor substrate and forming TCP wiring connecting the clock lines with the first shift register (see figures 2, 3; column 4, lines 6-15).

Regarding **claims 36** and **37,** in further discussion of claim 32, Kay teaches, Kay teaches how an input terminal 14 is configured to receive a signal sent from an input terminal of the second shift register 12 and from an output terminal of a previous stage $13_1$ (figure 12-14).

Also, Kay teaches how an output terminal of shift register $13_1$ is configured to output a signal to one of to an input terminal of a subsequent stage $13_2$ and to an output terminal $11_1$ of the second shift register 12 (figure 1 at $11_1$, $13_1$, $13_2$).

***Claim Rejections - 35 USC ' 103***

**4.** The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**5.** **Claims 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kay* (U.S. 6,175,352) in view of *Tanaka* (U.S. 5,369,417).

Regarding **claim 3,** in further discussion of claim 1, Kay does not teach how the first shift register would be a bi-directional shift register. On the other hand, Tanaka teaches this concept by teaching a sample and hold circuit that is suitably arranged for a source driver within a liquid

crystal panel wherein the first and second shift registers comprise bi-directional shift registers (column 8, lines 21-23).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Kay and Tanaka because while Kay teaches a shift register circuit comprising: a first shift register 21 having a plurality of stages connected in cascade (figure 1 at 21) and a second shift register 12 having more stages than the first shift register (figure 1 at 12, 21, column 3, lines 9-17), Tanaka teaches how such shift registers would be bi-directional shift registers (column 8, lines 21-23). The motivation for combining both inventions would have been to achieve a circuit within a display device that is capable of easily changing a phase relation of the shift clocks (column 3, lines 31-52).

6. **Claims 21-24, 30, 31, 33, 34** and **38-41,** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kay* (U.S. 6,175,352) in view of *Ishii et al* (U.S. 6,670,943).

Regarding **claims 33** and **34,** in further discussion of claim 32, Kay does not teach the concept of reducing a wiring resistance and capacitance of the clock lines by reducing a length and a line width of the clock lines. On the other hand, Ishii teaches this concept by teaching a driving circuit system for use in an active matrix display device (column 1, lines 5-11) wherein the pitch of the shift register can be increased such that the desired wiring resistance and capacitance of the clock lines would be achieved (column 19, lines 5-14).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Kay and Ishii because while Kay teaches a shift register circuit comprising: a first shift register 21 having a plurality of stages connected in cascade (figure 1 at 21) and a second shift register 12

having more stages than the first shift register (figure 1 at 12, 21, column 3, lines 9-17), Ishii teaches how to achieve the desired wiring resistance and capacitance of the clock lines (column 19, lines 5-14). The motivation for combining these inventions would have been to reduce the pixel pitch of the display device (column 3, lines 30-34).

Regarding **claims 21-24, 30, 31** and **38-41,** in further discussion of claims 1, 25 and 32, Kay does not teach how to divide the groups of shift registers with clock lines into odd and even groups. On the other hand, Ishii teaches this concept wherein the odd-numbered stages of the unit circuits LY1, LY3, . . . , which are numbered from the uppermost unit circuit, read an input signal at the rising edge of the clock signal CLY and output it, and the even-numbered stages of the unit circuits LY2, LY4, . . . , which are numbered from the uppermost unit circuit, read an input signal at the rising edge of the inverted clock signal CLY' and output it (column 16, lines 58 through column 17, lines 20).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Kay and Ishii because while Kay teaches a shift register circuit comprising: a first shift register 21 having a plurality of stages connected in cascade (figure 1 at 21) and a second shift register 12 having more stages than the first shift register (figure 1 at 12, 21, column 3, lines 9-17), Ishii teaches how to divide the groups of shift registers with clock lines into odd and even groups. The motivation for combining these inventions would have been to reduce the pixel pitch of the display device (column 3, lines 30-34).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,909,247 to *Hosokai et al* for a solid-state image pickup apparatus.

U.S. Patent 5,682,175 to *Kitamura* for a data driver generating two sets of sampling signals.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

09/28/2004

CHANH NGUYEN
PRIMARY EXAMINER